THAT WHICH IS CLAIMED IS:

1. A method of forming a semiconductor device comprising:

patterning a metal-gate layer and a gate polysilicon layer to form a gate pattern comprising a gate polysilicon pattern and a metal-gate pattern; and

covering at least a portion of a sidewall of the metal-gate pattern with an oxidation barrier layer, wherein the oxidation barrier layer comprises metal.

2. The method of claim 1, further comprising forming the oxidation barrier layer on the sidewall of the metal gate pattern using chemical vapor deposition (CVD) or an atomic layer deposition (ALD).

3. The method of claim 1, wherein the oxidation barrier layer comprises at least one of an oxide, nitride, or oxynitride of the metal.

4. The method of claim 3, wherein the oxidation barrier layer comprises a metal selected from the group consisting of aluminum (Al), tantalum (Ta), titanium (Ti), hafnium (Hf) and gold (Au).

5. The method of claim 1, further comprising sequentially forming a gate insulator layer, a gate polysilicon layer and a metal gate layer on a semiconductor substrate prior to the patterning step, wherein the covering step comprises depositing a metal layer and oxidizing or nitrifying the deposited metal layer.

6. The method of claim 1, wherein the oxidation barrier layer comprises aluminum oxide (Al_2O_3), and wherein the covering step comprises:

forming an aluminum layer using a CVD method by supplying methylpyrrolidine alane (MPA) as a source gas and argon (Ar) of 100sccm as a carrier gas at a temperature of between about 135~145°C and at a pressure of between about 0.1~1.1Torr; and

oxidizing the aluminum layer in an enriched oxygen environment.

7. The method of claim 1, wherein the oxidation barrier layer has a thickness of between about 5~100Å.

8. The method of claim 1, further comprising forming a barrier metal layer between the metal gate layer and the polysilicon layer, and wherein the gate pattern comprises a stacked gate polysilicon pattern, barrier metal pattern and metal gate pattern.

9. The method of claim 8, wherein the barrier and/or metal gate layer comprises tungsten.

10. The method of claim 7, wherein the barrier metal layer comprises tungsten nitride (WN) or titanium nitride (TiN).

11. The method of claim 7, wherein the oxidation barrier layer is selectively configured to cover substantially only the sidewall(s) of the metal gate layer and the barrier metal layer.

12. The method of claim 1, further comprising forming a capping layer on the metal-gate layer, wherein the capping layer is patterned when the metal-gate layer and the gate polysilicon layer are sequentially patterned, thereby forming a stacked gate pattern comprising, in serial order, a gate polysilicon pattern, a metal-gate pattern and a capping pattern.

13. The method of claim 12, further comprising forming a spacer layer to substantially cover a sidewall of the gate pattern including about: (a) the sidewall(s) of the polysilicon pattern; (b) the oxidation barrier layer over the metal-gate layer; and (c) the sidewall(s) of the capping pattern.

14. The method of claim 1, further comprising forming an impurity-doped region in the semiconductor substrate at opposing sides of the gate pattern using the gate pattern as an ion-implantation mask.

15. The method of claim 1, further comprising thermally treating the semiconductor substrate having the gate pattern with the oxidation barrier layer under an oxygen-enriched environment.

16. The method of claim 15, wherein the thermally treating under the oxygen-enriched environment comprises supplying nitrogen as a carrier gas comprising oxygen and hydrogen at a temperature of between about 750~950°C and a ratio of oxygen/hydrogen of between about 0.5~1.3.

17. A method of forming an integrated circuit device having a metal gate electrode comprising:

forming a stacked gate pattern onto a target substrate, the gate pattern comprising a metal-gate pattern with opposing first and second surfaces and at least one sidewall; and

covering at least a portion of the at least one sidewall of the metal-gate pattern with an oxidation barrier layer substantially without covering a sidewall of an adjacent gate polysilicon layer with the oxidation barrier layer.

18. A method according to Claim 17, wherein the covering the at least one sidewall of the metal-gate pattern comprises conformably covering substantially the entire outer surface of the sidewall(s) of the metal-gate pattern with the oxidation barrier layer.

19. A method according to Claim 18, wherein the gate pattern comprises a barrier metal layer abutting the metal-gate pattern, and wherein the covering step is carried out to also substantially cover the sidewall(s) of the barrier metal layer.

20. A method according to Claim 19, wherein the gate pattern comprises a plurality of stacked pattern components with at least one respective sidewall including a capping pattern above the metal-gate pattern and a gate polysilicon pattern below the metal-gate pattern, and wherein the gate pattern is substantially devoid of the

oxidation barrier layer proximate to the at least one sidewall of the respective gate polysilicon pattern and the capping pattern.

21. A method according to Claim 20, further comprising thermally treating the gate pattern in an oxygen-enriched environment and inhibiting an oxide layer from forming between the metal-barrier layer and the gate polysilicon layer based on the configuration of the oxidation barrier layer.

22. A method according to Claim 21, wherein the integrated circuit device is a highly integrated device with reduced gate pattern size, and wherein the oxidation barrier layer has a thickness of between about 5~100Å.

23. A method according to Claim 17, wherein the oxidation barrier layer comprises aluminum oxide (Al_2O_3), and wherein the covering step comprises:

forming an aluminum layer using a CVD method by supplying methylpyrrolidine alane (MPA) as a source gas and argon (Ar) as a carrier gas at a temperature above ambient; and

oxidizing the aluminum layer in an enriched oxygen environment to provide the oxidation barrier layer.

24. A method according to Claim 17, further comprising thermally treating the target substrate having the gate pattern with the oxidation barrier layer in an oxygen-enriched environment.

25. A method according to Claim 24, wherein the thermally treating under the oxygen-enriched environment comprises supplying nitrogen as a carrier gas comprising oxygen and hydrogen at a temperature of between about 750~950°C and a ratio of oxygen/hydrogen of between about 0.5~1.3.

26. A highly integrated semiconductor circuit device with metal gate electrodes and a reduced gate pattern size, comprising:

a substrate;

a gate insulation layer disposed over the substrate;

a plurality of spaced apart first gate patterns stacked on the gate insulation layer above the substrate;

a plurality of corresponding spaced apart metal barrier patterns, a respective one stacked on each of the first gate patterns above the gate insulation layer, the metal barrier patterns having at least one upwardly extending sidewall;

a plurality of corresponding second metal gate patterns, a respective one stacked on each of the metal barrier patterns above the first gate layer, the second metal gate patterns having at least one upwardly extending sidewall;

a plurality of corresponding capping patterns, a respective one stacked on each of the metal gate patterns above the metal barrier layer; and

an oxidation barrier layer conformably disposed over the metal barrier pattern sidewalls and the metal gate pattern sidewalls and being substantially absent on sidewalls of the first gate patterns and the sidewalls of the capping layer pattern, wherein the device is substantially devoid of an oxide layer extending at a boundary portion located between respective metal barrier patterns and the corresponding first gate layers.

27. A device according to Claim 26, wherein the oxidation barrier layer has a thickness of between about 5~100Å.